CS/EE181a: The ATHENA Microprocessor

November 6, 2013

1 Overview

The ATHENA microprocessor is an 8-bit harvard architecture microprocessor — it has one read only memory that stores instructions and a seperate read/write memory that stores its working data. Addresses are sent to the instruction memory over a 16-bit bus, and instructions are received over an 8-bit (one byte) bus. Most instructions are single byte instructions, but there are also a few 2 and 3 byte instructions. Such instructions must be received sequentially over the 8-bit instruction bus. The data memory has an 8-bit address bus, and 8-bit busses for data input and data output from the CPU. The instruction set supports up to eight 8-bit registers.

2 Chip IO

Both the instruction memory and the data memory are off chip devices. To save on the number of IO pins required on the CPU, there is a single 8-bit output bus and a single 8-bit input bus, and additional external hardware is needed to interface with the external memories, as can be seen in figure **??**. When the `addrselect` line is asserted, the value on the output bus is written to the external Address register. When the `datawrite` line is asserted, the value on the output bus is written to the data memory (the result will be undefined if the output bus chages while `datawrite` is asserted, so be sure to avoid this). The input bus is driven from the instruction memory when `memselect` is 0, and is driven from the data memory when `memselect` is 1. Both memories implement an asyncronous read, which means that when the memory address bus is updated, the input bus will not wait for any particular clock phase before updating its value.

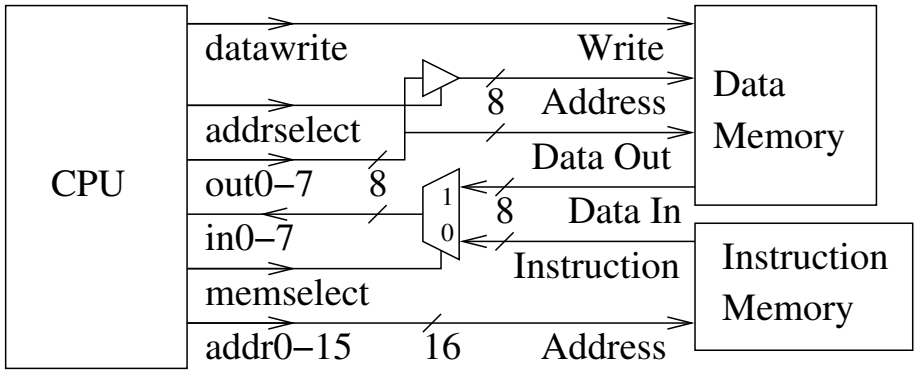

Figure 1: The ATHENA CPU and external components

3 Instruction Set

The instruction set supports up to 8 registers, which are usually refered to by number as registers 0 through 7. Register 0 is also known as the arithmetic accumulator, or register a. Register 1 is known as the logical accumulator, or register l. And register 2 is known as the shift register, or register s. The full instruction set is described in table **??**. All instructions also need to update the instruction memory address (also known as the program counter) upon completing the instruction. Unless otherwise specified, the program counter should be updated to point to the next instruction listed in the memory.

Instruction	First Byte	# of bytes	Descpition
MOV d, r	`11rrrddd`	1	Overwrite register d with value in register r
ADD a, r	`10rrr000`	1	Add register r to register a, overwriting register a
SUB a, r	`10rrr001`	1	Subtract register r from register a, overwriting register a
OUT r	`10rrr010`	1	Write the value in register r to the data memory
ADDR r	`10rrr011`	1	Write register r to the external address register
AND l, r	`10rrr100`	1	Bitwise AND of registers r and l, stored in register l
OR l, r	`10rrr101`	1	Bitwise OR of registers r and l, stored in register l
XOR l, r	`10rrr110`	1	Bitwise XOR of registers r and l, stored in register l
IN d	`01001ddd`	1	Read from data memory into register d
CIN d	`01010ddd`	2	Load 2nd instruction byte into register d
JMP	`00110000`	3	Set instruction address to the trailing instruction bytes
BRZ	`00101000`	3	If register l is zero, set instruction address as above
BRC	`00100100`	3	If the last ADD/SUB had the carry bit out of the top bit set, set the instruction address as in JMP above
LSR s	`00000010`	1	Shift value in register s to the right
ASR s	`00000011`	1	Shift value in register s to the right with sign extension

Table 1: The ATHENA instruction set