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; CS181 Test Part 1
; Written: Anjian Wu

; Assumed Constants
;   REG0        EQU     0x0H
;   REG1        EQU     0x1H
;   REG2        EQU     0x2H
;   REG3        EQU     0x3H
;   REG4        EQU     0x4H
;   REG5        EQU     0x5H
;   REG6        EQU     0x6H
;   REG7        EQU     0x7H



;   'Virtual' Data Memory
DATA    SEGMENT PUBLIC  'DATA'
                        ; Address
DB      00000001B       ; 0x0
DB      00000010B       ; 0x1
DB      00000011B       ; 0x2
DB      00000100B       ; 0x3
DB      ?               ; 0x4
DB      ?               ; 0x5
DB      ?               ; ... etc

; Instruction Memory, assume each OPERATION line is BYTE instruction/constant
; Commented and label do not count towards instruction
START:
;   Move immediate into Regs: Show memselect is correct with ASSERTS

    CIN     REG0
    00000000B
    CIN     REG1
    00000100B
    MOV     REG2, REG0
    MOV     REG3, REG1
    MOV     REG4, REG2
    MOV     REG5, REG3
    MOV     REG6, REG4
    MOV     REG7, REG5

;   Check writing to Data Memory and values are correct
    ADDR    REG7            ; Assert 00000100B, and assert addrselect is right
    OUT     REG0            ; Assert 00000000B, and assert addrselect is right
    OUT     REG1            ; Assert 00000100B, and assert addrselect is right
    OUT     REG2            ; Assert 00000000B, and assert addrselect is right
    OUT     REG3            ; Assert 00000100B, and assert addrselect is right
    OUT     REG4            ; Assert 00000000B, and assert addrselect is right
    OUT     REG5            ; Assert 00000100B, and assert addrselect is right
    OUT     REG6            ; Assert 00000000B, and assert addrselect is right
    OUT     REG7            ; Assert 00000100B, and assert addrselect is right

                                                        ; Reg Vals (* -> changed)
                                                        ; Reg0 = 00000000B*
                                                        ; Reg1 = 00000100B*
                                                        ; Reg2 = 00000000B*
                                                        ; Reg3 = 00000100B*
                                                        ; Reg4 = 00000000B*
                                                        ; Reg5 = 00000100B*
                                                        ; Reg6 = 00000000B*
                                                        ; Reg7 = 00000100B*

;   Logic/Arith Check and misc

    ADD     REG0            ; REG0 = 0
    ADD     REG1            ; REG0 = 00000100B = 4
    ADD     REG3            ; REG0 = 00001000B = 8
    ADD     REG5            ; REG0 = 00001100B = 12
    ADD     REG7            ; REG0 = 00010000B = 16
    OUT     REG0            ; Assert OUT = 00010000B

                                                        ; Reg Vals (* -> changed)
                                                        ; Reg0 = 00010000B*
                                                        ; Reg1 = 00000100B
                                                        ; Reg2 = 00000000B
                                                        ; Reg3 = 00000100B
                                                        ; Reg4 = 00000000B
                                                        ; Reg5 = 00000100B
                                                        ; Reg6 = 00000000B
                                                        ; Reg7 = 00000100B

    OR      REG0            ; REG1 = 00010100B
    OR      REG6            ; REG1 = 00010100B
    OUT     REG1            ; Assert OUT = 00010100B
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                                                    ; Reg Vals (* -> changed)
                                                    ; Reg0 = 00010000B
                                                    ; Reg1 = 00010100B*
                                                    ; Reg2 = 00000000B
                                                    ; Reg3 = 00000100B
                                                    ; Reg4 = 00000000B
                                                    ; Reg5 = 00000100B
                                                    ; Reg6 = 00000000B
                                                    ; Reg7 = 00000100B
XOR     REG5            ; REG1 = 00010000B
OUT     REG1            ; Assert OUT = 00010000B
                                                    ; Reg Vals (* -> changed)
                                                    ; Reg0 = 00010000B
                                                    ; Reg1 = 00010000B*
                                                    ; Reg2 = 00000000B
                                                    ; Reg3 = 00000100B
                                                    ; Reg4 = 00000000B
                                                    ; Reg5 = 00000100B
                                                    ; Reg6 = 00000000B
                                                    ; Reg7 = 00000100B
XOR     REG1            ; REG1 = 00000000B
OUT     REG1            ; Assert OUT = 00000000B
                                                    ; Reg Vals (* -> changed)
                                                    ; Reg0 = 00010000B
                                                    ; Reg1 = 00000000B*
                                                    ; Reg2 = 00000000B
                                                    ; Reg3 = 00000100B
                                                    ; Reg4 = 00000000B
                                                    ; Reg5 = 00000100B
                                                    ; Reg6 = 00000000B
                                                    ; Reg7 = 00000100B
SUB     Reg0            ; REG0 = 00000000B
OUT     REG0            ; Assert OUT = 00000000B
                                                    ; Reg Vals (* -> changed)
                                                    ; Reg0 = 00000000B*
                                                    ; Reg1 = 00000000B
                                                    ; Reg2 = 00000000B
                                                    ; Reg3 = 00000100B
                                                    ; Reg4 = 00000000B
                                                    ; Reg5 = 00000100B
                                                    ; Reg6 = 00000000B
                                                    ; Reg7 = 00000100B

SUB     REG5            ; REG0 = 11111100B
OUT     REG0            ; Assert OUT = 11111100B
                                                    ; Reg Vals (* -> changed)
                                                    ; Reg0 = 11111100B*
                                                    ; Reg1 = 00000000B
                                                    ; Reg2 = 00000000B
                                                    ; Reg3 = 00000100B
                                                    ; Reg4 = 00000000B
                                                    ; Reg5 = 00000100B
                                                    ; Reg6 = 00000000B
                                                    ; Reg7 = 00000100B

ADDR    REG4            ; Assert 00000000B, and assert addrselect is right
IN      REG6            ; REG6 = 00000001B
                                                    ; Reg Vals (* -> changed)
                                                    ; Reg0 = 11111100B
                                                    ; Reg1 = 00000000B
                                                    ; Reg2 = 00000000B
                                                    ; Reg3 = 00000100B
                                                    ; Reg4 = 00000000B
                                                    ; Reg5 = 00000100B
                                                    ; Reg6 = 00000001B
                                                    ; Reg7 = 00000100B

ADDR    REG6            ; Assert 00000001B, and assert addrselect is right
IN      REG4            ; REG6 = 00000010B
                                                    ; Reg Vals (* -> changed)
                                                    ; Reg0 = 11111100B
                                                    ; Reg1 = 00000000B
                                                    ; Reg2 = 00000000B
                                                    ; Reg3 = 00000100B
                                                    ; Reg4 = 00000010B
                                                    ; Reg5 = 00000100B
                                                    ; Reg6 = 00000001B
                                                    ; Reg7 = 00000100B
AND     REG0            ; REG1 = 00000000B
OUT     REG1            ; Assert OUT = 00000000B
                                                    ; Reg Vals (* -> changed)
                                                    ; Reg0 = 11111100B
                                                    ; Reg1 = 00000100B*
                                                    ; Reg2 = 00000000B
                                                    ; Reg3 = 00000100B
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                                                    ; Reg4 = 00000010B
                                                    ; Reg5 = 00000100B
                                                    ; Reg6 = 00000001B
                                                    ; Reg7 = 00000100B
AND     REG4            ; REG1 = 00000000B
OUT     REG1            ; Assert OUT = 00000000B

                                                    ; Reg Vals (* -> changed)
                                                    ; Reg0 = 11111100B
                                                    ; Reg1 = 00000100B*
                                                    ; Reg2 = 00000000B
                                                    ; Reg3 = 00000100B
                                                    ; Reg4 = 00000010B
                                                    ; Reg5 = 00000100B
                                                    ; Reg6 = 00000001B
                                                    ; Reg7 = 00000100B
```