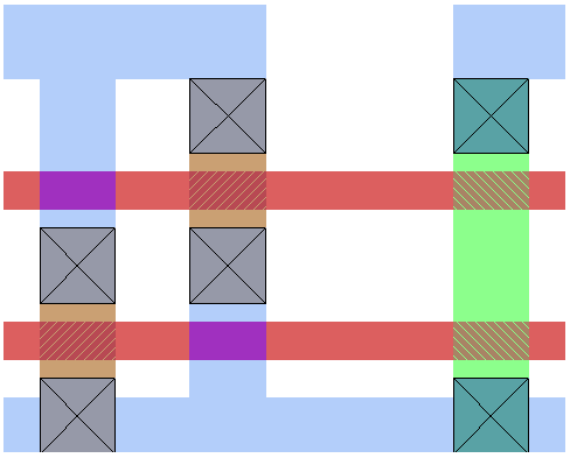
CS/EE 181
2013–14



`magic` layout of a NAND gate, a basic building block of CMOS circuitry.

Department of Computer Science
CALIFORNIA INSTITUTE OF TECHNOLOGY
Pasadena, California, U.S.A.

Welcome to CS/EE 181!

Teaching Staff for 2013/14:

Alain Martin <alain@async> 217 Ann.

Teaching Assistant:

Anjian Wu <wu.anjian@gmail.com>

Administrative Assistant:

Diane Goodfellow <diane@cs> 246 Ann.

System Manager:

David LeBlanc <unix-help@cs> 112 Ann.

Physical Resources

Class will meet in **Annenberg 243** Mondays and Wednesdays from **1** to **2:30** P.M.; exceptions will be announced well in advance.

You will be using computers in the computer lab on the first floor of **Annenberg**. These systems will be used for layout, simulation, and turning in assignments. A separate handout will cover the systems in more detail.

Course Requirements and Credits

CS/EE 181 is a 12-unit class and carries lab credit for EE and CS majors. No pass-fail!

The course consists of lectures and homework. The homework will consist of a mixture of short answer questions and laboratory work. Towards the end of the term, the emphasis of the assignments will shift to the individual term project.

Collaboration Policy

Students are expected to do their own work, but discussion of problem sets among classmates is allowed. However, students should do **all their own layout.** (Borrowing layout from cells provided by the instructors or from cells designed for an earlier assignment is permitted and encouraged.)

Grading Policy

Each homework assignment will be graded. Your final grade will be a weighted average of the grades that you received on the homework assignments and the final project. Your term grade is guaranteed to be *no worse* than that calculated from

50%(average of homeworks) + 50%(project grade).

Grading of individual assignments will be done on a 0–100 scale. The approximate meaning of homework scores is as follows:

0–49	F
50–59	D
60–74	C
75–89	B
90–99	A
100	A+

Late Policy

Unless you receive prior permission or have a verified illness, assignments completed late will be penalized 5% per day. Furthermore, the severity of any errors found will be multiplied by the number of days since the due date. The final score will be truncated at zero. Note that this algorithm will be applied on a per-problem basis. In other words, if you hand in half an assignment on time and the other half late, we shall apply the late penalty only to those problems that were turned late. *Please hand in what you have when the assignment is due and hand in the late part separately!*

Example 1.

John decided to go to a party rather than do his CS/EE 181 homework. As a result, he handed in all his answers one day late.

An impartial TA found a minor mistake and decided to take off 5%. Since the assignment was a day late, the total penalty was 5% + 5%, or 10%. The grade awarded would thus be 90% or approximately an **A**–. (Note that if John had gone to parties two nights in a row and handed in his CS/EE 181 assignment two days late, the penalty would have been 10% + 10% = 20%.)

Example 2.

Jack decided to go skiing rather than do his CS/EE 181 homework. When he got back, he felt too tired to do the entire assignment. As a result, he handed it in five days late with several errors.

A generous TA decided to only penalize Jack 20% for his errors. The total penalty came out to 5×5% + 5×20 % or 125%. This would yield a net total score of –25%, which truncates to zero, or an **F.**

The final rule is that any assignment not submitted by **2:45** P.M. **Friday, December 13, 2013** will be recorded as having received a grade of 0 (zero). (Special rules may apply to the project. If so, they will be announced well in advance!)

There will be no grades of "E" awarded in CS/EE 181 except in case of a documented medical emergency.

Fall Term Schedule CS/EE 181 2013–14

Sept. 30	Introduction to CS/EE 181 and VLSI
Oct. 2	Transistors, CMOS, and layout
Oct. 7	`magic` tutorial session (in lab)
Oct. 9	Boolean logic and transistor networks
Oct. 14	Logic minimization
Oct. 16	Clocks, timing, registers
Oct. 21	Precharge logic, domino logic, charge sharing, FSMs
Oct. 23	Computer arithmetic—Addition, subtraction
Oct. 28	Shifting, multiplication
Oct. 30	Putting it all together—planning a project
Nov. 4	Transistor physics
Nov. 6	Circuit performance, tau model—*Project proposal due*
Nov. 11	More circuit performance: Logical Effort
Nov. 13	Scaling and short-channel effects
Nov. 18	Power versus speed
Nov. 20	Metastability
Nov. 25	Wires
Nov. 27	Variability, reliability, NTV operation
Dec. 2	Memory
Dec. 4	Intro to asynchronous logic
Dec. 13	*Final project layout and report due*

Textbook

There is *no required text* for the course. The following books are on reserve on the first floor of Sherman Fairchild Library:

- Carver Mead and Lynn Conway. *Introduction to VLSI Systems.* Addison-Wesley, 1980. *(out of print)*
- Neil H. E. Weste and David Harris. *CMOS VLSI Design, A Circuits and Systems Perspective* fourth edition. Addison-Wesley, 2010.
- Zvi Kohavi. *Switching and Finite Automata Theory,* second edition. McGraw-Hill, 1970.

Class notes will be available in Diane Goodfellow's office for photocopying, on the Web, and may be handed out in lecture depending on the size of the class.

Fall Term Projects

Each student will individually design a CMOS chip, maximum 2x2 millimeters in SCMOS "scalable CMOS"(MOSIS *tinychip*, with design rules of a well-established technology. size) (This should mean a few thousand transistors, roughly a bit more complex than an 8-bit microprocessor, e.g., 6502 or AVR Tiny.)

- Start getting ideas for the project *now.*

- Projects that simulate correctly can be fabricated if you promise to test the chips.

Winter Term Activities

The winter term will cover asynchronous design, much in the style of CS 185, Asynchronous VLSI Design Laboratory.